Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE
_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES
_____

Ex parte BARTHOLOMEW BLANER AND
STAMATIS VASSILIADIS
_____

Appeal No. 97-1204
Application No. 08/453,948[1]
_____

ON BRIEF
_____

Before KRASS, FLEMING, and FRAHM, Administrative Patent
Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

_____

    [1] Application for patent filed May 30, 1995. According to
appellants, the application is a Division of Application No.
08/126,457, now U.S. Patent No. 5,465,377, issued November 7,
1995; which is a continuation of 07/642,011, issued January
15, 1991; now U.S. Patent No. 5,295,249.

Appeal No. 97-1204
Application No. 08/453,948

This is a decision on appeal from the final rejection of

claims 9 through 16, 24 and 25, all of the claims pending in

the application.

The invention is directed to the processing of

instructions for parallel execution. More particularly,

compounding tags are stored, along with the sequence of

instructions, in a cache.

Representative independent claim 9 is reproduced as

follows:

9.   In a digital computer system including means for
executing two or more instructions and a main memory and cache
for storing instructions, a method for processing instructions
for parallel execution, the method comprising the steps of:

storing a plurality of instructions in the main memory;
obtaining two or more instructions from the main memory for
execution;

in response to the two or more instructions, generating
compounding information signifying parallel execution of at
least two instructions; and

storing the at least two instructions and the compounding
information in the cache.

The examiner relies on the following references:

Pomerene et al. [Pomerene]   4,437,149   Mar. 13, 1984
Jardine et al. [Jardine]   5,075,844   Dec. 24,
1991

Appeal No. 97-1204
Application No. 08/453,948

                                        (filed May 24,
1989)

     Claims 9 through 16, 24 and 25 stand rejected under 35

U.S.C. 103 as unpatentable over Jardine in view of Pomerene.

     Reference is made to the brief and answer for the

respective positions of appellants and the examiner.

                              OPINION

We reverse.

     The examiner applies Jardine to the instant claims,

asserting that Jardine discloses everything but the details

about storing the sequence of instructions and the compounding

information in the cache memory. The examiner then relies on

Pomerene for an instruction compounding unit located between

the main memory and the cache, concluding that it would have

been obvious, within the meaning of 35 U.S.C. 103, to combine

the teachings as it would have

          allowed the Jardine's teachings to pre-compound
          (i.e. pre-decode) the instructions while
          transferring instructions from the main memory (i.e.
          slower memory) to the cache memory (i.e. faster
          memory), and store the pre-compounded instructions
          and the compounding information in the cache memory
          [answer-pages 5-6].

We agree with appellants that the examiner's reasoning is faulty for various reasons. While Jardine is clearly relevant to the claimed subject matter in permitting certain instructions to be executed in parallel, as can be seen in Jardine's Figures 1 and 7, the fetch unit 10 causes instructions to be stored in the instruction cache 12 and then processing is performed which will result in generating compounding information signifying parallel execution of at least two instructions. In the instant claimed invention, the generation of compounding information is done prior to storage of instructions and compounding information in the cache. In Jardine, any compounding information is generated downstream from the cache storage.

Further, as argued by appellants, the instant claimed subject matter requires that compounding tag information is stored in the cache along with the instructions. While the instant claims do not recite a "tag," explicitly, it is clear that this is what is being referred to by the "compounding information" [reference is made to the first paragraph of page 5 of the instant specification for a definition of "compounding" which involves the tagging process] in the

claims. Independent claims 9 and 24 make it clear that this
compounding information is stored in the cache along with the
instructions.

Thus, Jardine, alone, is clearly insufficient to cause
the instant claims to be unpatentable under 35 U.S.C. 103.
While the rejection is based on a combination of references,
we do not find Pomerene to remedy the deficiencies of Jardine,
as noted supra.

The basic error in the application of Pomerene to the
instant claims, as pointed out by appellants, is that Pomerene
is not directed to the execution of two or more instructions
or to a method for processing instructions for parallel
execution. Rather, Pomerene is concerned with the partial
decoding of instructions stored in a cache from the main
memory so that if and when said instruction(s) is/are called
from the cache by the processor, time is saved by the
processor not having to decode the instructions from scratch,
since the instructions are already partially decoded prior to
storage in the cache.

The examiner has equated this "partial-decoding" of
instructions by Pomerene to the claimed "compounding

information." Clearly, these operations are not the same nor

are they equivalent or even related. This is especially

apparent in view of appellants' definition of "compounding"

information appearing at page 5 of the instant specification.

No special information, or tag, is assigned, along with the

instructions stored in Pomerene's cache in order to determine

if two or more instructions may be executed in parallel.

Thus, we do not find the teachings of Pomerene to be

combinable with those of Jardine in any manner which would

arrive at the instant claimed subject matter.

The examiner's decision rejecting claims 9 through 16, 24

and 25 under 35 U.S.C. 103 is reversed.

No period for taking any subsequent action in connection

with this appeal may be extended under 37 CFR § 1.136(a).

<u>REVERSED</u>

ERROL A. KRASS   )
Administrative Patent Judge   )
)
)
)
) BOARD OF PATENT
MICHAEL R. FLEMING   )   APPEALS
Administrative Patent Judge   )   AND
) INTERFERENCES

6

```
                                    )
                                    )
                                    )
          ERIC FRAHM                )
          Administrative Patent Judge    )
```

lp

Appeal No. 97-1204
Application No. 08/453,948

LANE AITKEN AND MCCANN
2600 VIRGINIA AVENUE NW
WASHINGTON DC 20037

Leticia

Appeal No. 97-1204
Application No. 08/453,948

APJ KRASS

APJ FRAHM

APJ FLEMING

DECISION: <u>REVERSED</u>
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s): _____

Prepared: March 24, 2000

Draft   Final

3 MEM. CONF. Y   N

OB/HD   GAU

PALM / ACTS 2 / BOOK
DISK (FOIA) / REPORT